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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,969	08/06/2003	Bong-Hyun Kim	2522-024	1246

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,969	KIM ET AL.	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This office action is responsive to communication(s) filed on 12/22/04.

Claims 1-15, 17, 20-23 are pending.

Claims 1, 11, 20-23 have been amended.

2. Applicant's arguments with respect to independent amended claims 1, 11, 21 and other dependent claims 2-15, 17, 21-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4-6, 9-10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chang et al., U.S. Patent No. 6,380,029, in view of Tsukamoto et al., U.S. Patent No. 5,943,592.

Regarding claim 1, Chang et al. discloses a method of forming a gate in a non-volatile memory device comprising (See Fig. 2E-2F and Cols. 3-8):

. forming a tunnel dielectric layer 42 on a semiconductor substrate 40 (See Fig. 2E);

. forming a floating gate layer 44 on the tunnel dielectric layer;

. forming an integrate dielectric ONO layer 46 on the floating gate;

. forming a control gate layer 48 on the ONO layer;

. forming metal silicide 50 on the control gate;

. annealing the structure (line 67, Col. 7);

. patterning the silicide layer, control gate layer, the ONO layer, and the floating layer to form gate stack (Fig. 2F).

The control gate layer is formed comprising an in-situ doped silicon layer on the dielectric layer (doped silicon in CVD, lines 47-55, Col. 7).

However, Chang fails to disclose the step of forming the control gate comprising the steps of forming amorphous silicon layer on the integrate dielectric layer, thereafter, crystallizing the amorphous silicon layer by annealing the control gate layer.

Tsukamoto et al. discloses the method of forming a semiconductor device comprising: forming a floating layer 16 on the tunnel dielectric layer (12, 15), forming an integrate dielectric layer 17 over the floating gate layer, forming a control gate layer comprising the steps of forming doped amorphous silicon layer 18 over the integrate layer (Figs. 2B-2C), thereafter, crystallizing the amorphous silicon layer 18 by annealing

the control gate layer 18 to form crystallized silicon layer 21 (21, Fig. 2D; lines 59-63, Col. 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form control gate layer by forming amorphous silicon layer and then crystallizing the amorphous silicon layer because the control gate layer is formed by crystallizing the amorphous silicon layer to form polycrystal silicon layer would yield a greater grain size layer compare to polysilicon layer in order to reduce ions diffusion, thus suppress voltage fluctuation.

Regarding claim 2, Chang et al. and Tsukamoto et al. disclose the limitations of claim 1 and Chang further discloses the step of forming of floating gate layer comprises forming polysilicon (line 4, Col. 7).

Regarding claim 4, Chang et al. and Tsukamoto et al. disclose the limitations of claim 1 and Chang further discloses wherein the integrate dielectric layer comprises ONO (lines 18-20, Col. 7).

Regarding claims 5, 9-10, Chang et al. and Tsukamoto et al. disclose the limitations of claim 1, Chang et al. further discloses the control gate material is polysilicon and the annealing the control gate comprises RTA at temperature of about between 800-1000 oC (lines 47-67, Col. 7; RTA at 900 oC).

Regarding claim 6, Chang et al. and Tsukamoto et al. disclose the limitations of claim 1, Tsukamoto et al. further discloses wherein the control gate layer comprises amorphous silicon.

5. Claim 3 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Chang et al., U.S. Patent No. 6,380,029, in view of Tsukamoto et al., U.S. Patent No. 5,943,592, and further in view of Yeh, U.S. Patent No. 5,045,488.

Regarding claim 3, Chang et al. and Tsukamoto et al. disclose the limitations of claims 1 and 2, but fail to disclose wherein forming a floating gate layer comprises forming amorphous silicon. Yeh discloses the step of forming floating gate by forming amorphous silicon 22 (Fig. 3A) and then annealing the amorphous silicon to form polycrystal silicon floating gate (abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form floating gate layer by forming amorphous silicon layer and then crystallizing the amorphous silicon layer because the floating gate layer is formed by crystallizing the amorphous silicon layer to form polycrystal silicon layer would yield a greater grain size layer compare to polysilicon layer in order to reduce ions diffusion, thus suppress voltage fluctuation.

6. Claims 7-8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chang et al., U.S. Patent No. 6,380,029, in view of Tsukamoto et al., U.S. Patent No. 5,943,592, and further in view of U.S. Patent No. Zhang et al., U.S. Patent No. 6,413,805.

Regarding to claims 7-8, Chang et al. and Tsukamoto et al. disclose the limitations of claim 1 but fail to disclose wherein annealing the control gate layer comprises furnace annealing at a temperature of about 600-950 oC. Tsukamoto et al. discloses the annealing process if performed to crystallize the amorphous silicon layer at a temperature of about 650 oC (line 60, Col. 5). However, Zhang et al. discloses the use of furnace annealing to crystallize the amorphous silicon layer at the temperature that falls into the range cited in claim 8. It would have been obvious to one having ordinary skill in the art at the time the invention was made to anneal the amorphous silicon layer using furnace annealing because furnace annealing can heat the substrate at a lower temperature compare to other annealing process such as lamp or excimer laser, thus, avoiding the damage of the substrate.

7. Claims 11-14 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chang et al., U.S. Patent No. 6,380,029, in view of Yeh, U.S. Patent No. 5,045,488.

Regarding claim 11, Chang et al. discloses a method of forming a gate in a non-volatile memory device comprising (See Fig. 2E-2F and Cols. 3-8):

. forming a tunnel dielectric layer 42 on a semiconductor substrate 40 (See Fig. 2E);

. forming a first silicon layer as a floating gate layer 44 on the tunnel dielectric layer;

. forming an integrate dielectric ONO layer 46 on the floating gate;

. forming a second silicon layer as a control gate layer 48 on the ONO layer;

. forming metal silicide 50 on the control gate;

. annealing the structure (line 67, Col. 7);

. patterning the silicide layer, control gate layer, the ONO layer, and the floating layer to form gate stack (Fig. 2F).

Chang et al. fails to disclose the annealing process is furnace annealing. However, Yeh discloses the annealing process is furnace annealing. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use furnace annealing because furnace annealing can heat the substrate at a lower temperature compare to other annealing process such as lamp or excimer laser, thus, avoiding the damage of the substrate.

Regarding claim 12, Chang et al. and Yeh disclose the limitations of claim 11 and Chang further discloses the step of forming the first silicon layer comprises forming polysilicon (line 4, Col. 7).

Regarding claim 13, Chang et al. and Yeh disclose the limitations of claim 11 and Yeh further discloses the step of forming the first silicon layer comprising forming amorphous silicon 22 (Fig. 3A).

Regarding claim 14, Chang et al. and Yeh disclose the limitations of claim 11 and Chang further discloses the step of forming the second silicon layer comprises forming polysilicon.

8. Claim 15 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Chang et al., U.S. Patent No. 6,380,029, in view of Yeh, U.S. Patent No. 5,045,488, and further in view of Tsukamoto et al., U.S. Patent No. 5,943,592.

Regarding claim 15, Chang et al. and Yeh disclose the limitations of claim 11, but both fail to disclose wherein forming the second silicon layer comprises forming amorphous silicon. Tsukamoto et al. discloses the method of forming a semiconductor device comprising: forming a floating layer 16 on the tunnel dielectric layer (12, 15), forming an integrate dielectric layer 17 over the floating gate layer, forming a control gate layer comprising the steps of forming doped amorphous silicon layer 18 over the integrate layer (Figs. 2B-2C), and then crystallizing the amorphous silicon layer 18 by annealing the control gate layer 18 to form crystallized silicon layer 21 (21, Fig. 2D; lines 59-63, Col. 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form control gate layer by forming amorphous silicon layer and then crystallizing the amorphous silicon layer because the control gate layer is formed by crystallizing the amorphous silicon layer to form polycrystal silicon layer would yield a greater grain size layer in order to reduce ions diffusion, thus suppress voltage Vth fluctuation.

9. Claim 17 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Chang et al., U.S. Patent No. 6,380,029, in view of Yeh, U.S. Patent No. 5,045,488, and further in view of Zhang et al., U.S. Patent No. 6,413,805.

Regarding claim 17, Chang et al. and Yeh disclose the limitations of claim 11 but fail to disclose the temperature of furnace annealing is about 600-950 oC. Zhang disclose the furnace annealing is occurred at the temperature in the range cited in claim 17. It would have been obvious to one having ordinary skill in the art at the time the invention was made to anneal the amorphous silicon layer at low temperature of about 600-950 because furnace annealing at low temperature can heat the substrate at a lower temperature compare to other annealing process such as lamp or excimer laser or RTA, thus, avoiding the damage of the substrate and controlling the annealing process is much easier.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

12. Claims 20-23 are rejected under 35 USC 102 (a) as being anticipated by Chang et al., U.S. Patent No. 6,380,029.

Regarding claim 20, Chang et al. discloses a method of forming a gate in a non-volatile memory device comprising (See Fig. 2E-2F and Cols. 3-8):

. forming a tunnel dielectric layer 42 on a semiconductor substrate 40 (See Fig. 2E);

. forming a first silicon layer 44 on the tunnel dielectric layer;

. forming an integrate dielectric ONO layer 46 on the floating gate;

. forming a second silicon layer 48 on the ONO layer;

. forming metal silicide 50 on the second silicon layer;

. annealing the resultant structure (line 67, Col. 7);

. patterning the silicide layer, control gate layer, the ONO layer, and the floating layer to form gate stack (Fig. 2F).

Although Chang et al. doesn't mention the thickness variation of the ONO layer and a bird's beak at the interface between the ONO and the second silicon layer. It is inherent that when the second silicon is a crystallized material, the layer is not affected by thermal oxidizing process which resulting in bird's beak and variation of the thickness of the ONO layer. In other word, when the second silicon layer is a crystallized material, the variations of gate bird's beak is very small because of low impurity concentration occurred in crystallized silicon, producing no oxidation rate increasing effect, thus, variation of ONO layer is suppressed due to the reduction in the variation of the gate bird's beak.

Regarding claim 21, it is inherent that RTA is performed in an ambient including an inert gas.

Regarding claims 22-23, Chang et al. discloses wherein forming a metal silicide layer comprises using dichlorosilane gas to form a tungsten silicide layer (lines 57-63, Col. 7) and wherein the annealing is performed after forming the tungsten silicide layer (line 67, col. 7).

13. When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

14. For the above reasons, it is believed that the rejections should be sustained. Feature of an invention not found in the claims can be given no patentable weight in distinguishing the claimed invention over the prior art.

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date

of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1787. Other inquiries of this application should be called to (571) 272-1562 or the fax number (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao P. Le
Examiner
AU 2818